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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/687,475	10/16/2003	Ronald G. Filippi JR.	YOR920030441US1 (163-14)	7958

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EXAMINER	
ROSSOSHEK, YELENA	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 11/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/687,475	FILIPPI ET AL.
	Examiner	Art Unit
	Helen Rossoshek	2825

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11,13-21 and 23-30* is/are rejected.

7)☒ Claim(s) *12,22 and 31* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the Application 10/687,475 filed 10/16/2003.

2. Claims 1-31 are pending in the Application.

Claim Objections

3. Claims 11, 21 and 30 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. For example, claim 11 is a program storage device readable by machine cannot be dependent on claim 1, which is a method.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-11, 13-21 and 23-30 are rejected under 35 U.S.C. 102(e) as being anticipated by Lorenz et al. (US Application Publication 2005/0066301).

With respect to claim 1 Lorenz et al. teaches a method for analyzing circuit designs by using 3D numerical analysis of the governing partial differential equations

(PDE) (paragraph [0001]), wherein PDE analyses a discrete element model of the integrated circuit design (paragraph [0009]), comprising the steps of: discretizing a design representation into pixel elements representative of a structure in the design within generating a discrete element model 170 as shown on the Fig. 1A, wherein discrete element model 170 includes a mesh 171 created by mesh generator tool 145 out of integrated circuit design information including a schematic 130 (paragraph [0023]) and mesh represents components of the integrated circuit design (paragraph [0028]) and wherein the mesh representation is normally created by subdividing the geometric shapes that comprise the device into smaller simpler shapes called finite elements (paragraph [0006]); determining at least one property for each pixel element representing a portion of the design within creating the mesh representation of the corresponding components, wherein each component is characterized by parameter information, design information as fabrication process description and **material properties** (paragraph [0027]); and determining a response of the design due to local properties across the design within step 426 as shown on the Fig. 6, wherein the discrete element model including generated overall mesh created from individual meshes (step 424) is fed into a numerical solver to verify the assumptions made in creating the schematic of the integrated circuit or portion of it (paragraph [0034]).

With respect to claim 13 Lorenz et al. teaches a method for analyzing circuit designs by using 3D numerical analysis of the governing partial differential equations (PDE) (paragraph [0001]), wherein PDE analyses a discrete element model of the integrated circuit design (paragraph [0009]), comprising the steps of: discretizing a

design representation into pixel elements representative of a structure in the design within generating a discrete element model 170 as shown on the Fig. 1A, wherein discrete element model 170 includes a mesh 171 created by mesh generator tool 145 out of integrated circuit design information including a schematic 130 (paragraph [0023]) and mesh represents components of the integrated circuit design (paragraph [0028]) and wherein the mesh representation is normally created by subdividing the geometric shapes that comprise the device into smaller simpler shapes called finite elements (paragraph [0006]); analyzing properties in each pixel element within creating the mesh representation of the corresponding components, wherein each component is characterized by parameter information, design information as fabrication process description and **material properties** (paragraph [0027]), which are analyzed in the PDE solver for the analysis of the integrated circuit design (paragraph [0010]); assembling pixel properties to determine properties of a local three-dimensional circuit architecture within step 426 as shown on the Fig. 6, wherein the discrete element model including generated overall mesh created from individual meshes (step 424), wherein mesh is generated from 3D solid model derived from the schematic as shown on the Fig. 3 (paragraphs [0017], [0021]); and determining a global response of the circuit architecture due to local properties across the design by feeding the discrete-element model into a numerical solver to verify the assumptions made in creating the schematic of the integrated circuit or portion of it as shown in step 426 of the Fig. 6 (paragraph [0034]).

With respect to claim 23 Lorenz et al. teaches a method for analyzing circuit designs by using 3D numerical analysis of the governing partial differential equations (PDE) (paragraph [0001]), wherein PDE analyses a discrete element model of the integrated circuit design (paragraph [0009]), comprising the steps of: importing a digitally rendered representation of a design within the system-level design and design environment 110 shown on the Fig. 1A, which allows a user to digitally compose integrated circuit schematic using a graphical interface (paragraph [0022]); discretizing the design representation into pixel elements representative of a structure in the design within generating a discrete element model 170 as shown on the Fig. 1A, wherein discrete element model 170 includes a mesh 171 created by mesh generator tool 145 out of integrated circuit design information including a schematic 130 (paragraph [0023]) and mesh represents components of the integrated circuit design (paragraph [0028]) and wherein the mesh representation is normally created by subdividing the geometric shapes that comprise the device into smaller simpler shapes called finite elements (paragraph [0006]); analyzing properties in each pixel element by calculating the properties based on geometrical features in the design within creating the mesh representation of the corresponding components, wherein each component is characterized by parameter information including a **component's position, orientation, length, width, height**, design information as fabrication process description and material properties (paragraph [0027]), which are analyzed in the PDE solver for the analysis of the integrated circuit design (paragraph [0010]); assembling pixel properties in geometrical regions to determine properties of a local three-

dimensional circuit architecture within step 426 as shown on the Fig. 6, wherein the discrete element model including generated overall mesh created from individual meshes (step 424), wherein mesh is generated from 3D solid model derived from the schematic as shown on the Fig. 3 (paragraphs [0017], [0021]); and determining a global response of the circuit architecture due to the local properties across the design by feeding the discrete-element model into a numerical solver to verify the assumptions made in creating the schematic of the integrated circuit or portion of it as shown in step 426 of the Fig. 6 (paragraph [0034]).

With respect to claims 11, 21 and 30 Lorenz et al. teaches a program storage device readable by machine, tangibly embodying a program of instructions executable by the machine to perform method steps for analyzing circuit designs within conventional CAD system, wherein the mesh generators are computer instructions describing how to create a mesh for the associated component of the integrate circuit design (paragraph [0010]).

With respect to claims 2-10, 14-20, 24-29 Lorenz et al. teaches:

Claims 2, 14, 24: further comprising the step of exporting pixel properties to an application within the behavioral model and mesh generator associated with each component has share the same parameters and wherein the generator itself is a procedure that uses the parameter information (properties) (paragraph [0027]);

Claim 3: further comprising the step of assembling pixel properties to determine local three-dimensional properties within step 426 as shown on the Fig. 6, wherein the discrete element model including generated overall mesh created from individual

meshes (step 424), wherein mesh is generated from 3D solid model derived from the schematic as shown on the Fig. 3 (paragraphs [0017], [0021]) and within creating the mesh representation of the corresponding components, wherein each component is characterized by parameter information including a component's position, orientation, length, width, height, design information as fabrication process description and material properties (paragraph [0027]);

Claim 4: wherein the step of determining a response of the design due to local properties across the design includes the step of determining a global response for an architecture due to the local three-dimensional properties by feeding the discrete-element model into a numerical solver to verify the assumptions made in creating the schematic of the integrated circuit or portion of it as shown in step 426 of the Fig. 6 (paragraph [0034]), wherein creating the mesh representation of the corresponding components includes characterizing each component by parameter information including a component's position, orientation, length, width, height, design information as fabrication process description and material properties (paragraph [0027]);

Claims 5, 15: further comprising the step of importing a design to be analyzed within the system-level design and design environment 110 shown on the Fig. 1A, which allows a user to digitally compose integrated circuit schematic using a graphical interface (paragraph [0022]);

Claims 6, 16, 25 : wherein the design includes a computer generated design of one of a circuit and a chip within conventional CAD system, wherein the mesh

generators are computer instructions describing how to create a mesh for the associated component of the integrate circuit design (paragraphs [0010]; [0004]);

Claims 7, 17, 26: wherein the at least one property includes metal fraction and the global response includes thermal strain within creating the mesh representation of the corresponding components, wherein each component is characterized by parameter information, design information as fabrication process description and **material properties** (paragraph [0027]) and PDE solver is used to obtain 3D simulation results for at least on of mechanical, electrostatic, magnetic, thermal, **electrothermal**, piezoelectric, piezo-resistive, fluid damping and electromagnetic effects;

Claims 8, 18, 27: the step of determining a response of the design includes accepting or rejecting a design based on the response as shown in the example demonstrated by Fig. 5 depicting the result of analyzing the design, wherein mesh represents interconnections of a few beam components, which needs to be modified (rejecting a design based on the response) (paragraphs [0031]; [0033])

Claims 9, 19, 28: further comprising the step of altering a design based on the response within customizing the mesh generators by user in order to address specific geometrical requirements (paragraphs [0031], [0033]);

Claims 10, 20, 29: wherein the step of determining a response further includes representing a three-dimensional multi-layered design in two dimensions such that properties within all layers are accumulated and represented in the two-dimensional image as shown on the Fig. 4, wherein the comb components 212 in the schematic 200

are selected and autogenerated mesh 300 is created as two-dimensional image (paragraphs [0027], [0028]).

Allowable Subject Matter

6. Claims 12, 22 and 31 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art of record does not teach determination of the metal fraction as one of the properties of the individual mesh with indication of the number of stacked via structures as claimed.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Helen Rossoshek whose telephone number is 571-272-1905. The examiner can normally be reached on 7:00-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Examiner
Helen Rossoshek
AU 2825

STACY A. WHITMORE
PRIMARY EXAMINER